以太网分析仪 netANALYZER 在 EtherCAT 网络的测试举例

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以太网分析仪 netANALYZER 可以测试 profinet, EtherCAT, Ethernet/IP.sercos.Modbus/TCP 等实时和非实时网络, 主要有如下功能:

1.1、Data Recording-数据记录

可保存网络中所有的记录帧,可用 wireshark 等第三方工具打开;

1.2、Time Measurements-时序测试

可以分析报文帧出现的频率次数,以及通过设置不同的 port 端口来实现计算网络中不同位置点报文帧传输的时间,比如对 circle time 的测试,对 jitter 的测试等;

1.3、Analysis of Network Load

可以测试不同以太网帧帧在网络中的传输负载,可以图形化显示负载的变化规律;

1.4、其他参数

可测试以太网其他帧错误,见4.5小节

二、硬件介绍

24V 电源供电;

USB 接口: 可以插 U 盘保存记录;

Uplink 网口连接 PC, 作为数据传输网口连接 PC 端

TAP A 和 TAP B 共 4 路网口,两组网络,可实现同时对两路网络的测试; External IO 口,外扩 GPIO 口,可接远程 IO,实现对扩 IO 的信号抓取;



三、软件安装

Select netANALYZ	ER Device		—	
List of available d	evices			
Device Name	🔺 Туре		Serial No	
netANALYZER_0-192.	168 GbE		20033	
Scan for devi	ces Identi	fy (Blink)	Select	
netANALYZER				- 🗆 X
File Settings ?				
	TAP A		TAP B	
Status: STOPPED Link	TAP A Port 0 DOWN fix 100 Mbit/s	✓ Port 1 DOWN fix 100 Mbit/s	TAP B Port 2 DOWN fix 100 Mbit/s	✓ Port 3 DOWN fix 100 Mbit/s
Status: STOPPED Link Filter	TAP A Port 0 DOWN fix 100 Mbit/s ACTIVE	✓ Port 1 DOWN fix 100 Mbit/s ACTIVE	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE	✓ Port 3 DOWN fix 100 Mbit/s ACTIVE
Status: STOPPED Link Filter Transparent Mode	TAP A Port 0 DOWN fix 100 Mbit/s ACTIVE	Port 1 DOWN fix 100 Mbit/s ACTIVE	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE	Port 3 DOWN fix 100 Mbit/s ACTIVE
Status: STOFFED Link Transparent Mode	TAP A Fort 0 DOWN fix 100 Mbit/s ACTIVE	Port 1 DOWN fix 100 Mbit/s ACTIVE 0	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE 0	Port 3 DOWN fix 100 Mbit/s ACTIVE 0
Status: STOPPED Link Filter Transparent Mode Frames received OK Check sequence errors	TAF A Fort 0 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0	Port 1 POWN fix 100 Mbit/s ACTIVE 0 0 0 0	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE 0 0 0	Port 3 DOWN fix 100 Mbit/s ACTIVE 0 0 0
Status: STOPPED Link Filter Transparent Mode Frames received OK Check sequence errors Alignment errors WIL BY BE errors	TAP A Port 0 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Port 1 POWN fix 100 Mbit/s ACTIVE 0 0 0 0 0	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0	Port 3 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0
Status: STOFFED Link Filter Transparent Mode Frames received OK Check sequence errors Alignent errors MII EX_ER errors Short frames	TAP A	Port 1 POWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0	Port 3 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0
Status: STOFFED Link Filter Transparent Mode Frames received OK Check sequence errors Alignment errors MII RLER errors Short frames Frames too long	TAP A ✓ Port 0 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0 0 0 0	Port 1 POWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0 0 0 0 0	Port 3 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0
Status: STOFFED Link Filter Transparent Mode Frames received OK Check sequence errors Alignment errors MII RLER errors Short frames Frames too long Start of frame delimiter err	TAP A	✓ Port 1 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0 0 0 0 0	Port 3 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0
Status: STOPPED Link Filter Transparent Mode Frames received OK Check sequence errors Alignment errors MII RLER errors Short frames Frames too long Start of frame delimiter err Preamble too long	TAP A	✓ Port 1 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0 0 0 0 0	Port 3 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0 0 0
Status: STOFFED Link Filter Transparent Mode Frames received OK Check sequence errors Alignment errors Alignment errors Short frames Frames too long Start of frame delimiter err Freamble too long Preamble too short	TAP A	✓ Port 1 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0 0 0 0 0	<pre>Port 3 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</pre>
Status: STOFFED Link Filter Transparent Mode Frames received OK Check sequance errors Alignment errors Alignment errors MII RZER errors Short frames Frames too long Start of frame delimiter err Fremble too long Frames rejected by filter	TAP A	✓ Port 1 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0 0 0 0 0	Port 3 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Status: STOFFED Link Filter Transparent Mode Frames received OK Check sequence errors Aligment errors MII RLER errors Short frames Frames too long Start of frame delimiter err Freunble too long Freunble too short Frames rejected by filter Minimum Inter Frame Gap [ns]	TAP A Image: Point 0 Image: Point 0 </td <td>✓ Port 1 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0</td> <td>TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE</td> <td>✓ Port 3 DOWN fix 100 Mbit/s ACTIVE</td>	✓ Port 1 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0 0 0 0 0	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE	✓ Port 3 DOWN fix 100 Mbit/s ACTIVE
Status: STOPPED Link Filter Transparent Mode Frames received OK Check sequence errors Alignment errors MII RX_ER errors Short frames Frames too long Start of frame deliniter err Frames too long Start of frame deliniter err Frames too long Frames too long Branble too long Frames rejected by filter Minimum Inter Frame Gap [ns]	TAP A ✓ Port 0 DOWN fix 100 Mbit/s ACTIVE 0 0 0 0 0	✓ Port 1 DOWN fix 100 Mbit/s ACTIVE 0 0 0	TAP B Port 2 DOWN fix 100 Mbit/s ACTIVE	✓ Port 3 DOWN fix 100 Mbit/s ACTIVE

四、EtherCAT 测试步骤

分别测试了 KPA EtherCAT master 和以及其他主站的, 硬件接线如下图, 使用了 TAP A 的 port0 和 port1, 主站网口--->port0--->port1--->从站伺服



4.1Data Recording-数据记录功能

4.1.1 设置过滤条件:

0 Fort 1 Fort 2 Fort 3

此处并不设置任何过滤条件, 全部 EtherCAT 的报文帧都会被抓取下来, port0 和 port1 的设置都一致, 设置完成后需要点击 apply to all。

🗯 netAl	NALYZER				– 🗆 🗙	
File	Settings ?					
	File Settings			TAP B		
Stat	GPIO Settings		Port 1	Port 2	Port 3	
	Filters Settings		DOWN fix 100 Mbit/s	DOWN fix 100 Mbit/s	DOWN fix 100 Mbit/s	
	PHY Settings Extended Software	Filters Settings	ACTIVE	ACTIVE	ACTIVE	
	Analysis Configurati	ion				
Franë	s received UK	003	803		0	
Check	sequence errors	0	0	0	0	
Aligne	ment errors	0	0	0	0	
MII R	X_ER errors	0	0	0	0	
Short	frames	0	0	0	0	
Frame	s too long	0	0	0	0	
Start	of frame delimiter err	0	0	0	0	
Pream	ble too long	0	0	0	0	
Press	ble too short	0	0	0	0	
Frame	s rejected by filter	0	0	0		
Wester	Tatur Burge Car []	960	960			
Minimo	um inter Frame Gap [ns]			10 8	10 8	
	Bus Load %	0	0	0	0	
R	ecording Time: 00:00:00 h	Capture Data	~	Start	tConvert	
Status: Ca	apture Data ready				GPIO: Start/Stop manua	
		- 0	X Filter Settings			
			Fort C Filters	2 Fort 3		
Save		Select Filter Apply t	e All	aT fromas	Save ilter A	Mable Filter B
Filter A	Enable F	ilter B	-LWR	index offset	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7 A	index offset Ox0 Dx1 C
# 0x0 0x1 0x2 0x1	0 0x4 0x5 0x6 0x7 ^ index offset	0x0 0x1 0x2 0x3 0x4 0x5 0x6	0x7 CLWR0b	0±000 Valu	00 00 00 00 00 00 00	0±000 Value 00 00
(Besk00 00 00	00 00 00 00	(00 00 00 00 00 00 00 00	-LWR1	0.000 11.1	00 00 00 00 00 00 00	0.000 101 00 00



4.1.2 选择数据记录功能

netANALYZER				– 🗆 X
File Settings ?				
-	TAP A		TAP B	
Status: STOPPED	✓ Port 0 UP 100 Mbit/s	✓ Port 1 UP 100 Mbit/s	Port 2 DOWN fix 100 Mbit/s	✓ Port 3 DOWN fix 100 Mbit/s
Filter Transparent Mode	ACTIVE	ACTIVE	ACTIVE	ACTIVE
Frames received OK	803	803	0	0
Check sequence errors	0	0	0	0
Alignment errors	0	0	0	0
MII RX_ER errors	0	0	0	0
Short frames	0	0	0	0
Frames too long	0	0	0	0
Start of frame delimiter err	0	0	0	0
Preamble too long	0	0	0	0
Preamble too short	0	0	0	0
Frames rejected by filter	0	0	0	0
Minimum Inter Frame Gap [ns]	960	960	n/a	n/a
Bus Load %	0. 726	0.726	0	0
Recording Time: 00:00:00 h	Capture Data	~	Start	Convert
tatus: Capture Data ready				GPIO: Start/Stop manua

4.1.3 导出抓包数据

可以通过 wirshark 等第三方软件工具打开



4.1.4 测试结果

🛅 cnc-1000us_00001	2018/8/10 16:53	Wireshark capture f	1,534 KB
CNT0_00001	2018/8/9 14:38	Wireshark capture f	2,631 KB
Default_00001	2018/8/9 13:51	Wireshark capture f	2,631 KB
LWR_00001	2018/8/9 16:58	Wireshark capture f	4,267 KB
modbus123_00001	2018/8/10 15:19	Wireshark capture f	1,078 KB
💼 robot-500us_00001	2018/8/10 16:06	Wireshark capture f	5,928 KB
🗋 x86-maixin-1000us_00001	2018/8/13 15:04	Wireshark capture f	726 KB
💼 zynq-maixin_00001	2018/8/14 9:38	Wireshark capture f	5,082 KB

4.2.Time Measurements-时序测试

4.2.1 设置过滤条件

参考 4.1.1 设置过滤条件如下,比如设置 LWR 报文指令,位置如下

<pre>bitterCAT Trame neader EtherCAT datagrams(s): 4 EtherCAT datagrams: Cm Header Cmd : 10 (Index: 0x21 Log Addr: 0x00011 Bilength : 6 (0 Interrupt: 0x0000 Data: 00000000000 bata: 00000000000 bata: 00000000000 BilterCAT datagram: Cm Header Cmd : 11 (</pre>	:00_00 Cmds, d: 'LRU Logica 000 x6) - M d: 'LWF Logica	00 D1 :00:0 D' (1 Rea No Ro R' (1 Wri	<pre>ts), 0 (0 ': 1 0), d) undt 1), te)</pre>	85 0:00 en 0 Len	by 0:0 6, : 6 - 1	tes 0:00 'LWM , AM	ca 0:0 R': ddr e F ddr	ptu 0:0 le 0x oll	rec 0), n 6 110 ows	i (e Ds i, ' 000,	ERD	oits) Broad : 10 : 0) dcas en 1	st I	(ff:	:ff 1w'	:ff : 1	:ff en 3	:ff 8	:ff)
Index: 0x21 Log Addr: 0x00012	000 x6) - M	NO RO	undt	rin		Mor	0 E	011	ows											
0000 ff ff ff ff ff ff fi 00 000	0 00 0 6 80 0 1 00 0 0 00 4 9 08 0	00 00 00 00 06 80 40 00 00 00	00 00 01 00	00 8 00 0 00 0 80 0 00 0	88 : 00 0 00 0 00 0	a4 4 00 0 00 2 00 0	45 00 23 00 00	10 00 d2 00 00				@.		E. #.				_		;
ort 0 Port 1 Port 2 Port 3	1				_															
ort 0 Port 1 Port 2 Port 3	Cop Z Enab	py ble Filt	Ser A	ave							🗹 En	able F	ilter	[в] Sel	.ect :	Filte	r Apj	ply t	o All
ort 0 Port 1 Port 2 Port 3 Filters HitherCAT All EtherCAT frames LWR0b	Cop Enab index	py ble Filt offset O	ser A z0 Oz1	ave 0x2	0x3	0x4	0x5	0x6	0x7	^	En index	able F	ilter 0x0	[B 0x1	Sel Ox2	ect Ox3	Filte	r Ap	ply t Ox6	• All 0x7
ort 0 Port 1 Port 2 Port 3 ☐ FilterS ☐ FilterCAT ↓ LWROb ↓ LRW	Cop Enable index Cop 0x000	py ble Filt offset O Valu <mark>g</mark>	ser A x0 0x1	ave 0x2 00	0x3 00	0x4 00	0x5	0x6 00	0x7 00	^	En index 0x00	able F offset O Val	ilter OxO	B 0x1 00	0x2	ect Ox3 00	Filte Ox4 OO	r Ap: 0x5	ply t Ox6 OO	• All 0x7 00
Drt 1 Port 2 Port 3 Port 1 Port 3 Port 3 Port 3 Drt 0 Port 1 Port 3 P	Cop Enable index ⁰ 0x000 0x008	py ble Filt offset 0 Value (de Values	Ser A x0 0x1 0 00 5ax200	0x2 00 00	0x3 00 00	0x4 00	0x5 00	0x6 00 00	0x7 00 00	-	En index 0x00	able F offset 0 Val 8 Val	ilter OxO Oğus	B 0x1 00 200	Sel 0x2 00 00	0x3	Filte 0x4 00 00	r Ap: 0x5 00 00	0x6	• All 0x7 00 00
Port 1 Port 2 Port 3 Filters Filters LWR0 LWR0 LWR0 LWR0	Coy Coy index 0x000 0x008	py ble Filt offset O Valu Valu 0 Valu 0 0	ser Å x0 0x1 0 00 3ax200 0 00 fax200	0x2 00 00 00	0x3 00 00 00	0x4 00 88 FF	0x5 00 00 A4 FF	0x6 00 00 00	0x7 00 00 00		En index 0x00	able F offset 0 Val 8 Val	ilter 0x0 08es u€00	B 0x1 00 200 00	Sel 0x2 00 00 00	ect 0x3 00 00 00	Filte 0x4 00 00 00	r Ap: 0x5 00 00 00	ply t 0x6 00 00 00	• All 0x7 00 00 00
Port 1 Port 2 Port 3 Filters Filters Fullers	Cop Enab index ⁰ 0x000 0x008 0x008	py ble Filt offset O Valugo Valugo Valugo	ser A x0 0x1 0 00 0 00 0 00 0 00 0 00	0x2 00 00 00 00 00	0x3 00 00 00 00	0x4 00 88 FF 00	0x5 00 A4 FF 00	0x6 00 00 00 00	0x7 00 00 00 00		En index 0x00 0x00	able F offset O Val 8 Val 0 Val	ilter 0x0 0844 0844 0844 0844 0844 0844	B 0x1 00 300 00 300 00	Sel 0x2 00 00 00 00 00	0x3 00 00 00 00 00	Filte 0x4 00 00 00 00 00	r Ap: 0x5 00 00 00 00	0x6 00 00 00 00 00	• All 0x7 00 00 00 00 00
ort 0 Port 1 Port 2 Port 3 ⇒ Filters ⇒ EthercAT → LWR → LWR	Cog Enab index 0 0x000 0x008 0x010	py ble Filt offset 0 Valu 0 Valu 0 Valu 0 0	ser A x0 0x1 0 00 0 00 0 00 1 x2 0 00 1 x2 0 00 1 x2 0 00 1 x2 0 00 1 x2 0 00 1 x2 0 0 1 x2 0 0 0 0 1 x2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x2 00 00 00 00 00	0x3 00 00 00 00 00	0x4 00 88 FF 00 00	0x5 00 84 FF 00	0x6 00 00 00 00 00	0x7 00 00 00 00 00		En index 0x00 0x00	able F offset 0 Val 8 Val 0 Val	ilter 0x0 0845 0845 0845 0845 0845 0845	B 0x1 00 00 00 00 00	0x2 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00	r App 0x5 00 00 00 00 00	0x6 00 00 00 00 00 00	• All 0x7 00 00 00 00 00 00
Prt 1 Port 2 Port 3 Fillers EtherCAT LWR 0b LWR 0b LWR 0b UWR 10 UWR 10 UWR 10 EtheretPOWERLINK Modus/TCP	Cop Enab index © 0x000 0x008 0x010 0x010	py ble Filt offset 0 Valu 0 Valu 0 Valu 0 Valu 0 Valu 0	ser A x0 0x1 0 00 5x200 0 00 5x200 0 00 5x200 0 00 5x200 0 00	0x2 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00	0x4 00 88 FF 00 00	0x5 00 A4 FF 00 00	0x6 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00		✓ En index 0x00 0x00 0x01	able F offset 0 Val 8 Val 0 Val 8 Val	ilter 0x0 084 084 084 084 084 084 084 084 084 08	0x1 0x1 00 00 00 00 00 00	0x2 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00	r Ap; 0x5 00 00 00 00 00 00 00	0x6 00 00 00 00 00 00 00 00	 All 0x7 00
rt 0 Port 1 Port 2 Port 3 → Fillers → Fillers → All EtherCAT → All EtherCAT frames → LWR 0 → LWR 0 → LWR 1 → LWR 1 → LWR 1 → EthereLIVE ↔ EthereLIVE ↔ EthereLIVE ↔ EthereLIVE ↔ ModbusTCP ↔ Sercos III → Sercos III → EthereLIVE → Sercos III → Sercos III	Cop ✓ Enab index ° 0x000 0x008 0x010 0x010	py ble Filt offset 0 Valu 0 Valu 0 Valu 0 Valu 0 0 Valu 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Ser A 20 0x1 00 00 00 00 00 00 00 00 00 0	ave 0x2 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00	0x4 00 88 FF 00 00 00 00	0x5 00 84 FF 00 00 00 00	0x6 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00		✓ En index 0x00 0x00 0x01 0x01	able F offset 0 Val 8 Val 0 Val 8 Val	ilter 0x0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	B 0x1 00 200 200 200 200 200 200 200	Sel 0x2 00	0x3 00 00 00 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00 00 00 00	r App 0x5 00 00 00 00 00 00 00 00 00	Ply t 0x6 00 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00 00 00
rt 0 Port 1 Port 2 Port 3 Fillers Fillers FillerCAT All EherCAT All EherCAT LWR UWR0b LRW LWR0b LRW EherCAT EherCAT EhereNIP EhereNIP EhereNIP EhereNIP Forestat Secos II User defined	Cop ✓ Enat index ⁶ 0x000 0x010 0x010 0x018 0x020	py ble Filt offset 0 Valu Valu Valu Valu 0 Valu 0 Valu 0 Valu 0 Valu	ser A 20 021 0 00 0	0x2 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00	0x4 00 88 FF 00 00 00 00	0x5 00 A4 FF 00 00 00 00	0x6 00 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00		✓ En index 0x00 0x01 0x01 0x01 0x01	able F offset 0 Val 8 Val 0 Val 8 Val	ilter 0x0 080 084 084 084 084 084 084 084 084 08	B 0x1 00 00 00 00 00 00 00 00 00 00	Sel 0x2 00	0x3 00 00 00 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00 00 00 00 00	r Ap: 0x5 00 00 00 00 00 00 00 00 00 00 00	Ply t 0x6 00 00 00 00 00 00 00 00 00 00	All Ox7 O
rt 0 Port 1 Port 2 Port 3 Fillers Fil	Cop ✓ Enat index ⁶ 0x000 0x010 0x010 0x018 0x020	ey ble Filt offset 0 Valu 0 Valu 0 Valu 0 Valu 0 Valu 0 Valu 0 0 Valu 0	Seer A 20 02:1 0 00 0	ave 0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00	0x4 00 88 FF 00 00 00 00 00 00	0x5 00 44 FF 00 00 00 00 00 00	0x6 00 00 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00 00		✓ En index 0x00 0x00 0x01 0x01 0x01	able F offset 0 Val 8 Val 8 Val 8 Val	ilter 0x0 080 080 080 080 080 080 080 080 080	B 0x1 00 00 00 00 00 00 00 00 00	Sel 0x2 00 00 00 00 00 00 00 00 00 00 00 5F	0x3 00 00 00 00 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00 00 00 00 00 00	r Ap; 0x5 00 00 00 00 00 00 00 00 00 00 00	0x6 00 00 00 00 00 00 00 00 00 00 00	All Ox7 O
rt 0 Port 1 Port 2 Port 3 Pillers LWR0 LWR0 LWR0 LWR0 LWR0 EthereNP EthereNP EthereNP EthereNP EthereNP USer defined Port 1 Port 3	Cop	Py ble Filt offset 0 Valu Valu Valu Valu Valu Valu Valu Valu	x0 0x1 3x2 0x1 3x2 0x1 3x2 00 3x2 00 00 3x2 00 00 00 00 00 00 00 00 00 00	ave 0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00 00	0x4 00 88 FF 00 00 00 00 00 00 00	0x5 00 84 FF 00 00 00 00 00 00 00	0x6 00 00 00 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00 00 00		✓ En index 0x00 0x00 0x01 0x01 0x01 0x02 0x02	able F offset 0 Val 8 Val 8 Val 0 Val	ilter 0x0 08ax 08ax 00 08ax 00 08ax 00 08ax 00 08ax 00 08ax	B 0x1 00 00 00 00 00 00 00 00 00 00 00 00	Sel 0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00 00 00 00 00 00 00	r Ap; 0x5 00 00 00 00 00 00 00 00 00 00 00 00 00	Ply t 0x6 00 00 00 00 00 00 00 00 00 00 00 00 00	All Ox7 O
rt 0 Port 1 Port 2 Port 3 Fillers Fillers Fillers Fillers Fillers FillerCAT FillerCAT frames FillerCAT FillerCATALL Fi	Cop	Py ble Filt offset 0 Valu 0 Valu 0 Valu 0 Valu 0 Valu 0 Valu 0 Valu 0 0 Valu 0 0 Valu 0 0 Valu 0 0 0 0 0 0 0 0 0 0 0 0 0 0	xer A x0 0x1 1 0 0 1 0	0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00	0x4 00 88 FF 00 00 00 00 00 00 00 00 00	0x5 00 84 FF 00 00 00 00 00 00 00 00	0x6 00 00 00 00 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00 00 00 00		✓ En index 0x00 0x01 0x01 0x01 0x02 0x02	able F offset 0 Val 8 Val 0 Val 0 Val 8 Val	ilter 0x0 08as u00 08as u00 08as u00 08as u00 08as u00 08as u00 08as	B 0x1 00 00 00 00 00 00 00 00 00 00 00 00	Sel 0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00 00 00 00 00 00 00	r App 0x5 00 00 00 00 00 00 00 00 00 00 00 00 00	Ply t 0x6 00 00 00 00 00 00 00 00 00 00 00 00 00	All All Ox7 O
rt 0 Port 1 Port 2 Port 3 Fillers Fillers FillerCAT All EberCAT frames UWR UWR UWR UWR UWR UWR EberCAT ALL EbernerUP E	Cog Enait index ⁶ 0x0000 0x008 0x010 0x018 0x020 0x028 0x028 0x030	ey ble Filt offset Valu 0 Valu 0	xer A x0 0x1 x0 0x1 x0 0x x0 0 x x0 x	ave 0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	0x4 00 88 FF 00 00 00 00 00 00 00 00 00 00 00 00	0x5 00 84 FF 00 00 00 00 00 00 00 00 00 00	0x6 00 00 00 00 00 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00 00 00 00 00 00		En E	able F offset 0 Val 8 Val 0 Val 8 Val 8 Val	ilter 0x0 08a 08a 08a 08a 08a 08a 08a 08a 08a 08	B 0x1 00 00 00 00 00 00 00 00 00 00 00 00 00	Sel 0x2 00	ect : 0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00 00 00 00 00 00 00	r App 0x5 00 00 00 00 00 00 00 00 00 00 00 00 00	Ply t 0x6 00 00 00 00 00 00 00 00 00 00 00 00 00	All All Ox7 O
ort 0 Port 1 Port 2 Port 3 Filters Filters FilterCAT All EberCAT frames -UWR -UWR0b -LWR1 -UWR1 -UWR1 EberCAT-ALL EbereatPOWERLINK Modbus/CP PROFINET Sercos III User defined	Con Enak index ⁶ 0x0000 0x008 0x000 0x010 0x010 0x020 0x022 0x028 0x028	ey view of the second s		ave 0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	0x4 00 88 88 FF 00 00 00 00 00 00 00 00 00 00 00 00	0x5 00 84 FF 00 00 00 00 00 00 00 00 00 00 00 00	0x6 00 00 00 00 00 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00 00 00 00 00 00		En En Contractor	able F offset 0 Val 8 Val 0 Val 8 Val 8 Val	ilter 0x0 084 084 084 084 084 084 084 084 084 08	B 0x1 00 00 00 00 00 00 00 00 00 00 00 00 00	Sel 0x2 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00 00 00 00 00 00 00	r App 0x5 00 00 00 00 00 00 00 00 00 00 00 00 00	Ply t 0x6 00 00 00 00 00 00 00 00 00 00 00 00 00	All Ox7 O
rt 0 Port 1 Port 2 Port 3 Prillers EtherCAT UWR0 UWR0 UWR0 UWR0 EthereWP EthereWP EthereWP EthereWP USerdefined User defined	Cog ✓ Enat index * 0x000 0x010 0x018 0x020 0x028 0x028 0x030	ey view of the second s		0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	0x4 00 00 00 00 00 00 00 00 00 00 00 00 00	0x5 00 A4 FF 00 00 00 00 00 00 00 00 00 00 00 00	0x6 00 00 00 00 00 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00 00 00 00 00 00		 ✓ En Index 0x00 0x01 0x01 0x02 0x02 0x03 0x03 0x03 	able F offset 0 Val 8 Val 0 Val 8 Val 8 Val 0 Val 8 Val	ilter 0x0 084 084 084 084 084 084 084 084 084 08	B 0x1 00 00 00 00 00 00 00 00 00 00 00 00 00	Sel 0x2 00	ect 2 0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00 00 00 00 00 00 00	r Ap; 00 00 00 00 00 00 00 00 00 0	ply t 0x6 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	All Dx7 O
ort 0 Port 1 Port 2 Port 3 Fillers Fillers FillerGAT All EtherCAT frames UWR0b UWR0b UWR0b UWR0 UWR0 UWR0 EthernetP0 EtherneP0 EthernetP0 EthernetP0 EthernetP0 EthernetP0 EthernetP0 E	Cog ✓ Enat Index ⁶ 0x000 0x008 0x010 0x010 0x010 0x020 0x020 0x020 0x020 0x030	By Sile Filt O Value Value Value Value Value Value Value Value Value		0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	0x4 00 00 00 00 00 00 00 00 00 00 00 00 00	0x5 00 A4 FF 00 00 00 00 00 00 00 00 00 00 00 00	0x6 00 00 00 00 00 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00 00 00 00 00 00		 ✓ En Index 0x00 0x01 0x01 0x02 0x02 0x03 0x03 0x03 	able F offset 0 Val 8 Val 0 Val 8 Val 0 Val 8 Val 0 Val	ilter 0x0 084 084 084 084 084 084 084 084 084 08	B 0x1 00 00 00 00 00 00 00 00 00 00 00 00 00	Sel 0x2 00	eet 2 0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00 00 00 00 00 00 00	r Ap; 00 00 00 00 00 00 00 00 00 0	Ply t 0x6 00 00 00 00 00 00 00 00 00 0	All Ox7 Ox7 O
prt 0 Port 1 Port 2 Port 3 → Filters → ElflerGAT → All EbrerCAT frames → UWR 0 → UWR	Cog Trat Index C 0x000 0x010 0x010 0x010 0x020 0x0	By Sile Filt O Value O	See A x0 0x1 0 00 0 0	0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	0x4 00 88 FF 00 00 00 00 00 00 00 00 00 00 00 00	0x5 00 84 7F 00 00 00 00 00 00 00 00 00 00 00 00 00	0x6 00 00 00 00 00 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00 00 00 00 00 00		 ✓ En Index 0x00 0x01 0x01 0x02 0x02 0x03 0x03 0x04 0x04 0x04 0x05 0x04 <	able F offset 0 Val 8 Val 0 Val 8 Val 0 Val 8 Val 0 Val 8 Val	ilter 0x0 054 054 054 054 054 054 054 054 054 05	B 0x1 00 00 00 00 00 00 00 00 00 00 00 00 00	Sel 0x2 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00 00 00 00 00 00 00	r Ap: 0x5 00 00 00 00 00 00 00 00 00 00 00 00 00	Ply t 0x6 00 00 00 00 00 00 00 00 00 00 00 00 00	All Ox7 O
<pre>prt 0 Port 1 Port 2 Port 3 Filters Filters FilterCAT FilterCAT FilterCAT FilterCAT FilterCAT FilterCAT FilterCAT FilterCATALL FilterCATAL FilterFilterCATALL FilterCATALL FilterCATAL</pre>	Cog ✓ Enat index ⁶ 0x000 0x008 0x010 0x018 0x020 0x028 0x030 0x030 0x038 0x030	py Valu of Valu of Val	see A x x 0 x	0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	0x4 00 88 FF 00 00 00 00 00 00 00 00 00 00 00 00	0x5 00 A4 FF 00 00 00 00 00 00 00 00 00 00 00 00	0x6 00 00 00 00 00 00 00 00 00 00 00 00 00	0x7 00 00 00 00 00 00 00 00 00 00 00 00 00		 ✓ En Index 0x00 0x01 0x01 0x02 0x02 0x03 0x03 	able F offset 0 Val 8 Val 0 Val 8 Val 0 Val 8 Val 0 Val	ilter 0x0 054 054 054 054 054 054 054 054 054 05	B 0x1 00 00 00 00 00 00 00 00 00 00 00 00 00	Sel 0x2 00 00 00 00 00 00 00 00 00 00 00 00 00	0x3 00 00 00 00 00 00 00 00 00 00 00 00 00	Filte 0x4 00 00 00 00 00 00 00 00 00 00 00 00 00	r Ap: 0x5 00 00 00 00 00 00 00 00 00 00 00 00 00	Dx6 0x6 00	0 A11 00 00 00 00 00 00 00 00 00 00 00 00 0

4.2.2 选择时序测试功能

在弹出来的时序图,可根据不同端口 port 的设置来确定不同参数的设置,比如 from port0 to port0,是用来测试 circle time。

InetANALYZER				- 🗆 X
File Settings ?				
Status:	TAP A	_	TAP B	
STOPPED	✓ Port 0 UP 100 Mbit/s	⊻ Port 1 UP 100 Mbit/s	✓ Port 2 DOWN fix 100 Mbit/s	✓ Port 3 DOWN fix 100 Mbit/s
Filter	ACTIVE	ACTIVE	ACTIVE	ACTIVE
🗌 Transparent Mode				
Frames received OK	803	803	0	0
Check sequence errors	0	0	0	0
Alignment errors	0	0	0	0
MII RX_ER errors	0	0	0	0
Short frames	0	0	0	0
Frames too long	0	0	0	0
Start of frame delimiter err	0	0	0	0
Preamble too long	0	0	0	0
Preamble too short	0	0	0	0
Frames rejected by filter	0	0	0	0
Minimum Inter Frame Gap [ns]	960	960	n/a	n/a
Bus Load %	0. 726	0.726	0	0
Recording Time: 00:00:00 h	Timing Analysis	~	Start	Reset
Status: Timing Analysis ready				GPIO: Start/Stop manua



4.2.3 测试结果

改图横坐标是 circle time, 纵坐标是采样次数, 可以看出, 如果 circle time 不抖动的话, 是 一根直线, 如果存在抖动的话, 会呈现一个类似正态分布的图像











其他主站-1000us



其他主站-4ms

4.3.Analysis of Network Load-网络负载

4.3.1 设置过滤条件

首先需先将 Filter Setting 下的过滤条件打钩去掉, 然后新增加额外的过滤条件如下, 比如我 需要查看 EtherCAT 报文的负载情况, 我设置过滤条件如下



Stat File Settings GPIO Settings Filters Settings PHY Settings PHY Settings Analysis Configuration Fract received OK Analysis Configuration Fract received OK Check sequence errors 0 Alignment errors 0 Short frames 0 Start of frame deliniter err 0 Premest to long 0 Premes too long 0 Premes too long 0 Premes too long 0 Premes rejected by filter 0 Pus Load % 0 0 Pus Load % 0 Capture Data ready Add Filter Entry	File Settings ?			Extended Software Filters	
Recording Time: 00:00:00 h stus: Capture Data tus: Capture Data ready Add Filter Entry Clear Tree	Stat GPIC Settings File Settings GPIC Settings Filters Settings PHY Settings PHY Settings PHY Settings Check sequence errors Alignment errors MII RX_ER errors Short frames Frames too long Start of frame delimiter err Preamble too long Preamble too short Frames rejected by filter Minimum Inter Frame Gap [ns] Bus Load %	Filters Settings on 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Port 1 DOWN fix 100 NG ACTOP	Filter Tree	3 44 HERDAT
Add Filter Entry Clear Tree	Recording Time: 00:00:00 h	Capture Data	~		
	tus: Capture Data ready			Add Filter Entry -	Clea <u>r</u> Tree

4.3.2 选择网络负载功能

ile Settings ?	 .			
Shahura'	TAP A		TAP B	
STOPPED	Port 0	Port 1	Port 2	Port 3
Link	UP 100 Mbit/s	UP 100 Mbit/s	DOWN fix 100 Mbit/s	DOWN fix 100 Mbit/
Filter	ACTIVE	ACTIVE	ACTIVE	ACTIVE
Transparent Mode				
Frames received OK	0	0	0	
Check sequence errors	0	0	0	
lignment errors	0	0	0	
MII RX_ER errors	0	0	0	
Short frames	0	0	0	
Frames too long	0	0	0	
Start of frame delimiter err	0	0	0	
Preamble too long	0	0	0	
Preamble too short	0	0	0	
Frames rejected by filter	0	0	0	
Minimum Inter Frame Gap [ns]	0	0	0	
Bus Load %	0	0	0	
Recording Time: 00:00:00 h	Netland Analysis	~	Start	: Convert

4.3.3 测试结果



4.4 其他参数

通过测试界面,	可以查看到网络中会出现一些诊断错误信息。
T netANAI	VZER

M NELANALYZEK				- ^
File Settings ?				
Status: RUN Link	TAP A Port 0 UP 100 Mbit/s	VP 100 Mbit/s	TAP B Port 2 DOWN fix 100 Mbit/s	✓ Port 3 DOWN fix 100 Mbit/s
Filter	ACTIVE	ACTIVE	ACTIVE	ACTIVE
Transparent Mode	1			
Frames received OK	1981456	1981456	0	0
Check sequence errors	250	210	0	0
Alignment errors	103	159	0	0
MII RX_ER errors	12534	10259	0	0
Short frames	250	210	0	0
Frames too long	0	0	0	0
Start of frame delimiter err	12391	10064	0	0
Preamble too long	12219	9894	0	0
Preamble too short	400	316	0	0
Frames rejected by filter	61270	61247	0	0
Minimum Inter Frame Gap [ns]	1080	1120	n/a	n/a
Bus Load %	0.871	0.871	0	0
Recording Time: 00:33:01 h	Timing Analysis	\sim	Stop	Reset
Status: Timing Analysis in progres	s			GPIO: Start/Stop manua

五、其他测试例子

以上例子都是基本使用和基本测试的方法,其他测试例子可以参考以下几个应用例子做对应 的测试;

5.1 双通道接线测试



5.2 双通道独立接线测试



5.3 带有 GPIO 信号输入测试

